ABSTRACT

The objective of the present invention is to provide a data transfer control device and electronic equipment that guarantee stable operation even if a reset that clears the node topology information occurs. When a CPU (firmware) of a data transfer control device in accordance with the IEEE 1394 standard issues a data transfer start (or resume) command during a bus reset period, the execution of that command is canceled. The fact that the command has been canceled is informed to the CPU by an interrupt. The command is canceled by using a signal that is active during the bus reset period to mask a signal that goes active when a command is issued. When a pause command is issued, the transfer processing pauses at a previously determined pause location. Transfer data is automatically divided into a series of packets to be transferred continuously by the hardware. When a resume command and a pause command for transfer data have been issued together, the CPU executes the transfer processing in steps then pauses the transfer processing.